

# MS-7038

Version 0B  
11/12/2003 Update

Intel (R) Springdale (GMCH) + ICH5 Chipset  
Intel Northwood & Prescott mPGA478B Processor

## CPU:

Intel Northwood/Prescott - 3.0G & Above

## System Chipset:

Intel Springdale - GMCH (North Bridge)  
Intel ICH5 (South Bridge)

## On Board Chipset:

CLOCK -- Cypress CY28405

## On Board Chipset:

BIOS -- FWH EEPROM 4M  
AC'97 Codec -- REALTEK ALC655  
LPC Super I/O -- W83627THF  
LAN - REALTEK RTL8110S/8100C

## Main Memory:

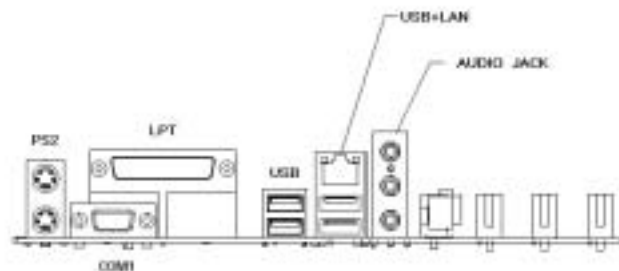
DDR \* 2 (Max 4GB)

## Expansion Slots:

PCI2.3 SLOT \* 3  
AGP4X/8X SLOT \* 1

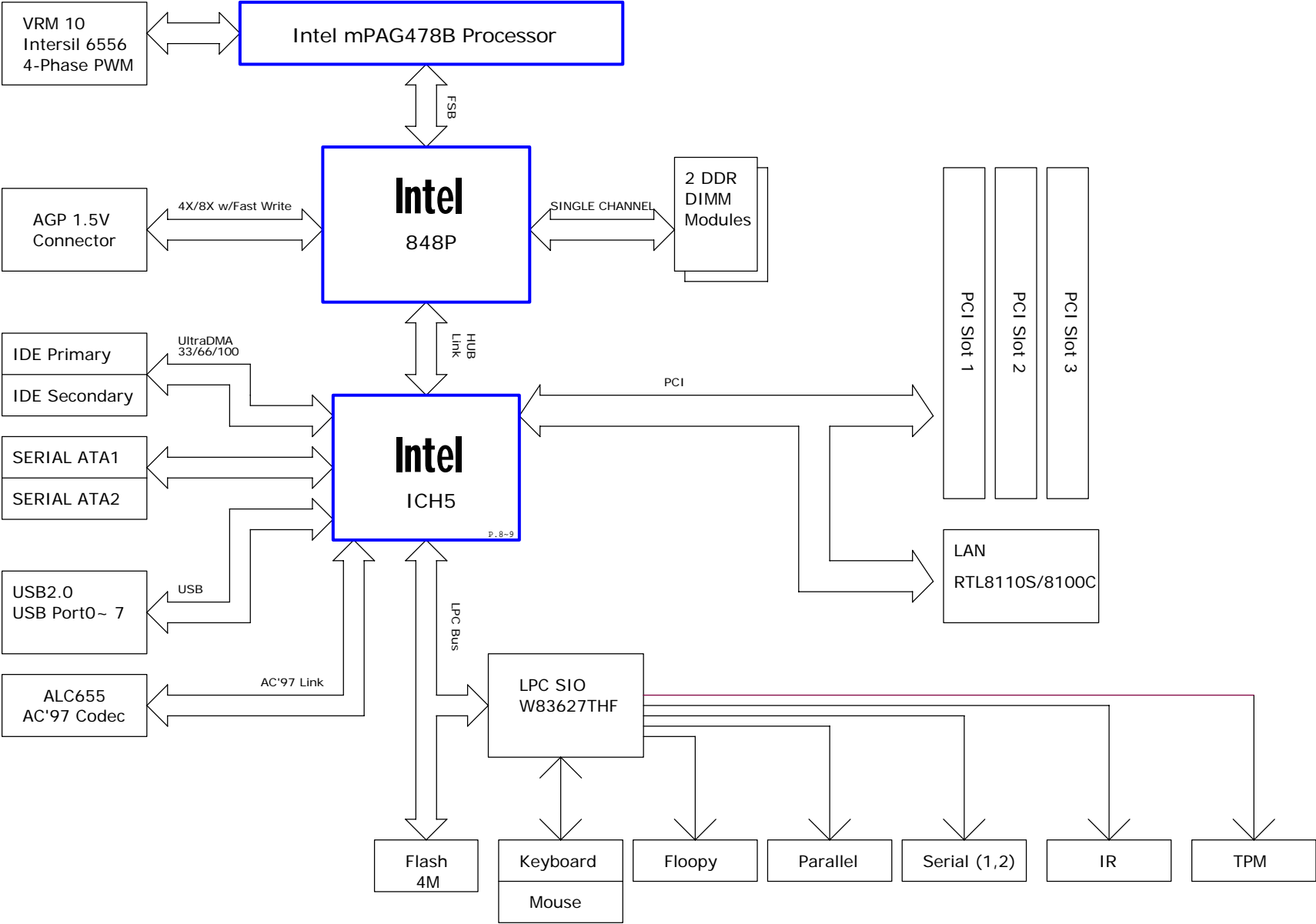
## Intersil PWM:

Controller: HIP6556A  
Driver: HIP6602B \* 2  
FMB 1.5 SPEC.

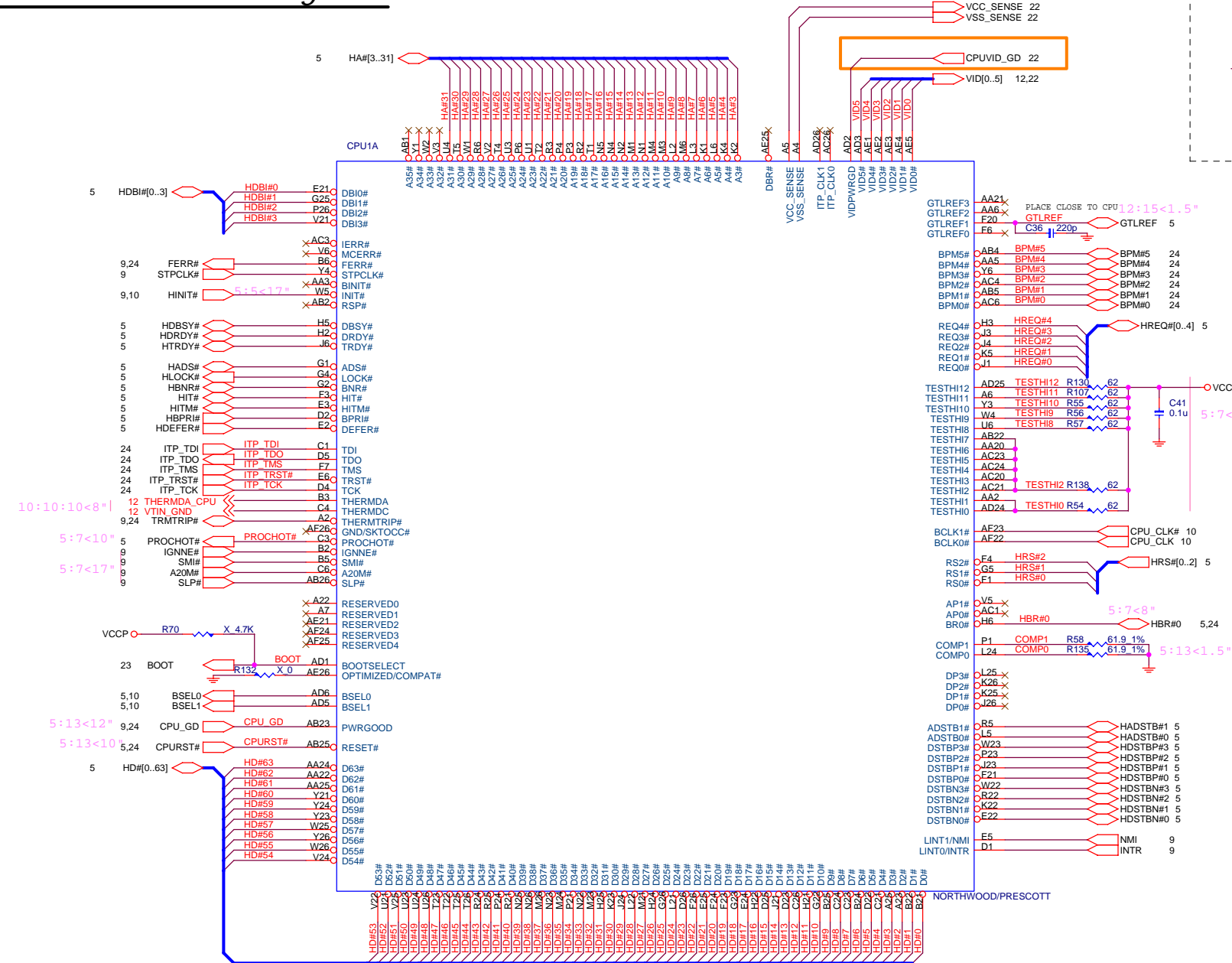


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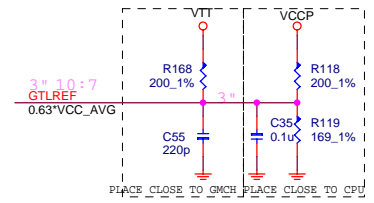
# Block Diagram



# Intel mPGA478B - Signals

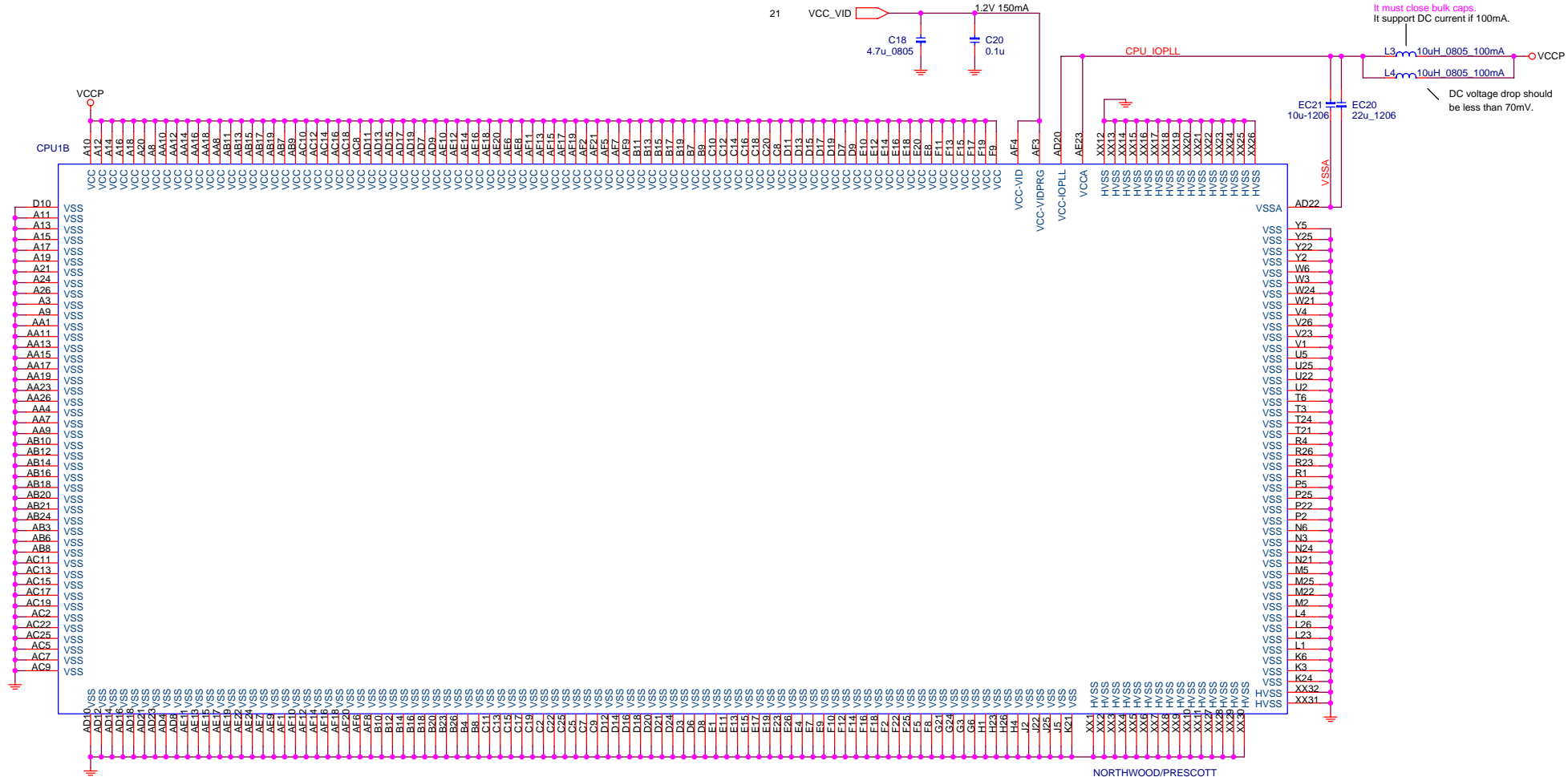


## CPU GTL REFERENCE VOLTAGE BLOCK

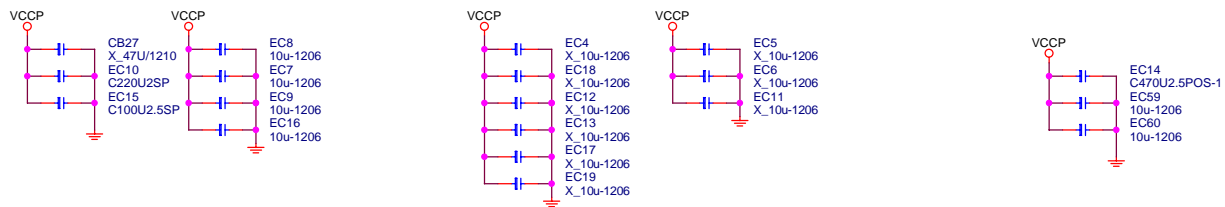


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Intel mPGA478B - Signals		
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Intel mPGA478B - Power



CPU DECOUPLING CAPACITORS



4pcs Place these caps within socket cavity

19pcs Place these caps within north side of processor

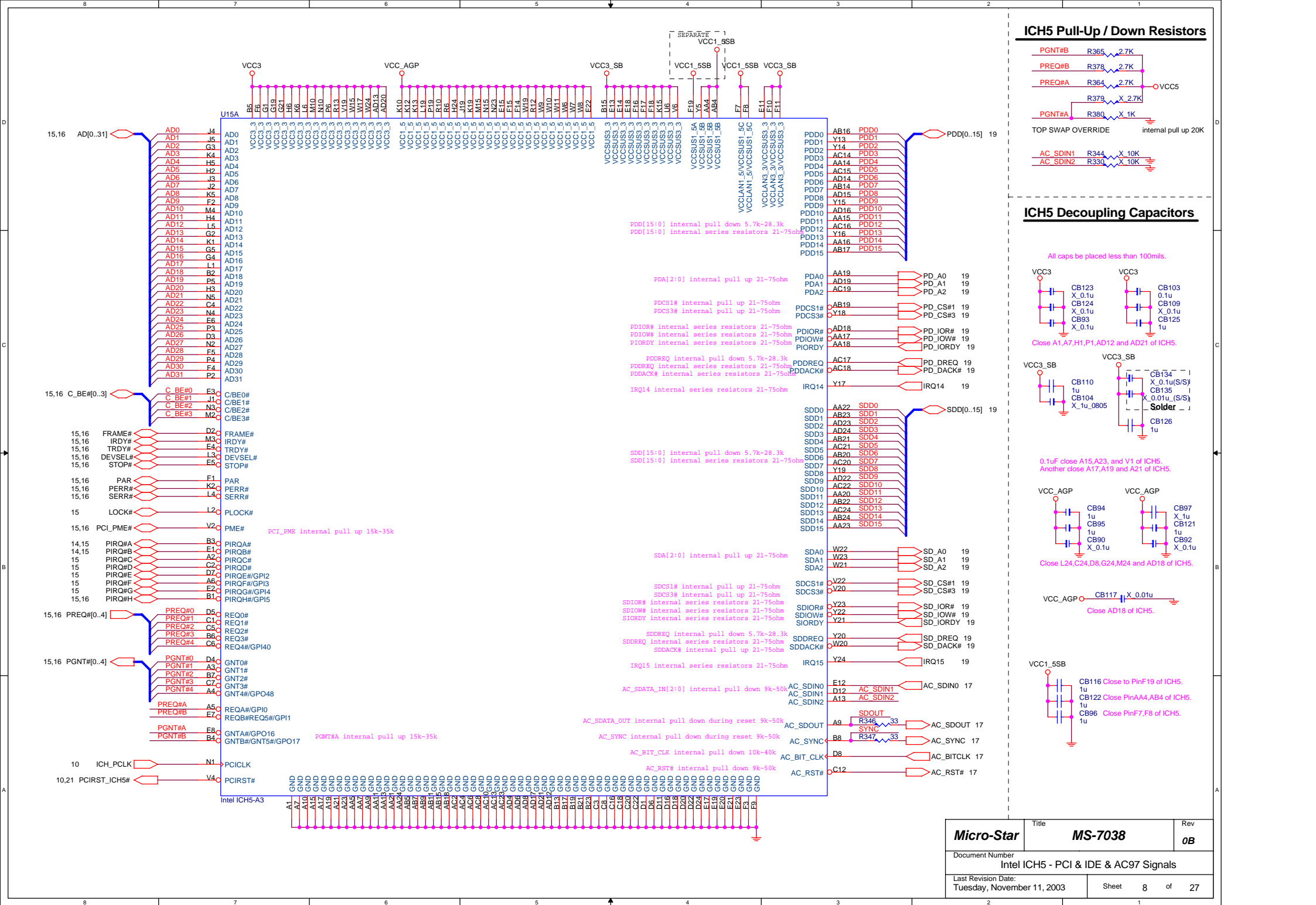
9pcs Place these caps within south side of processor

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## DDR DIMM1

## SIGNALS

## POWER

ADDR.=1010000B(A0H)

## DDR DIMM2

## SIGNALS

## POWER

ADDR.=1010001B(A2H)

## DDR Termination Resistors

## SIGNALS

## POWER

Place these decoupling capacitors close to VTT\_DDR termination resistors.  
One decoupling capacitor for each R-pack.

Micro-Star	Title	MS-7038	Rev	0B
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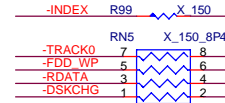
# LPC SUPER I/O W83627HF/THF

FANIO3 FANIO3 14

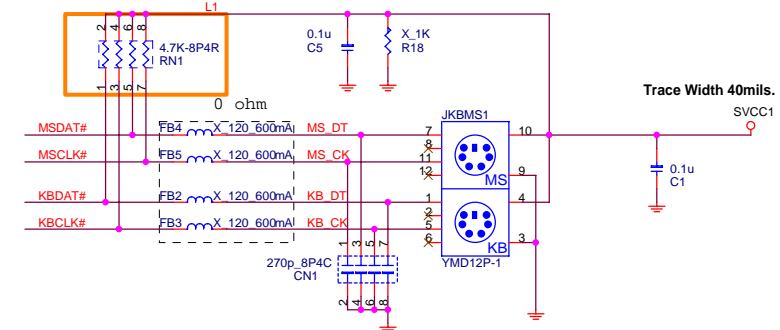
## FLOPPY CONNECTOR

## SUPER I/O STRAPPING RESISTOR

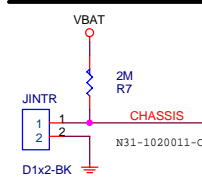
VCC5	R48	4.7K	SOUTA
VCC5	R8	4.7K	SOUTB
VCC5	R4	4.7K	
VCC5	R73	4.7K	RTSA#
SOUTA	L: Disable KBC	H: Enable KBC	
SOUTB	L: 24MHZ	H: 48MHZ	
RTSA#	L: CFAD=2E	H: CFAD=4E	
DTRA#	L: PNP Default	H: PNP no Default	



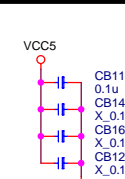
## PS2 KEYBOARD & MOUSE CONNECTOR



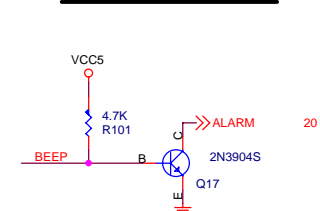
## Chassis Intrusion



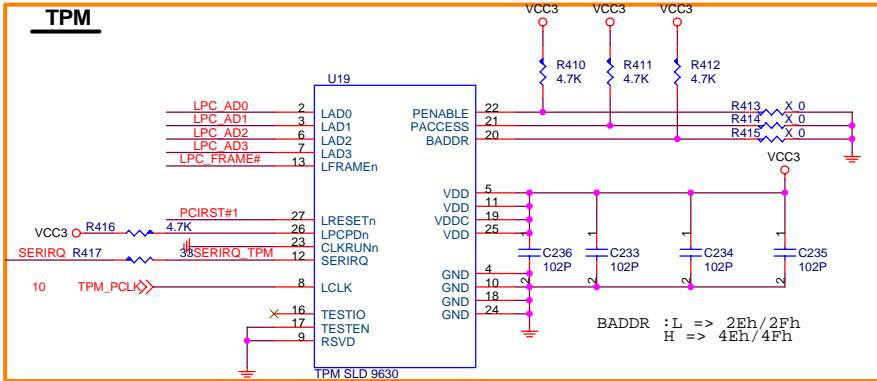
## DECOUPLING CAPACITORS



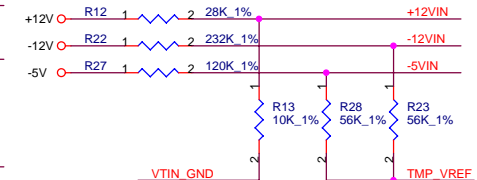
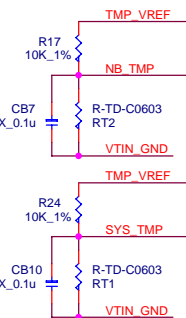
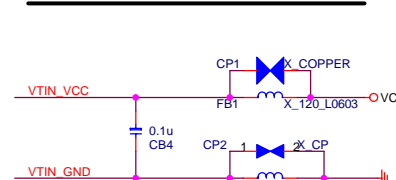
## SPEAKER BLOCK



## TPM



## THERMAL RESISTOR BLOCK



NOTE: LOCATE CLOSE STATUS PANEL

Micro-Star	Title	MS-7038	Rev	0B
Document Number	SIO-W83627THF & KB/MS & FDD			
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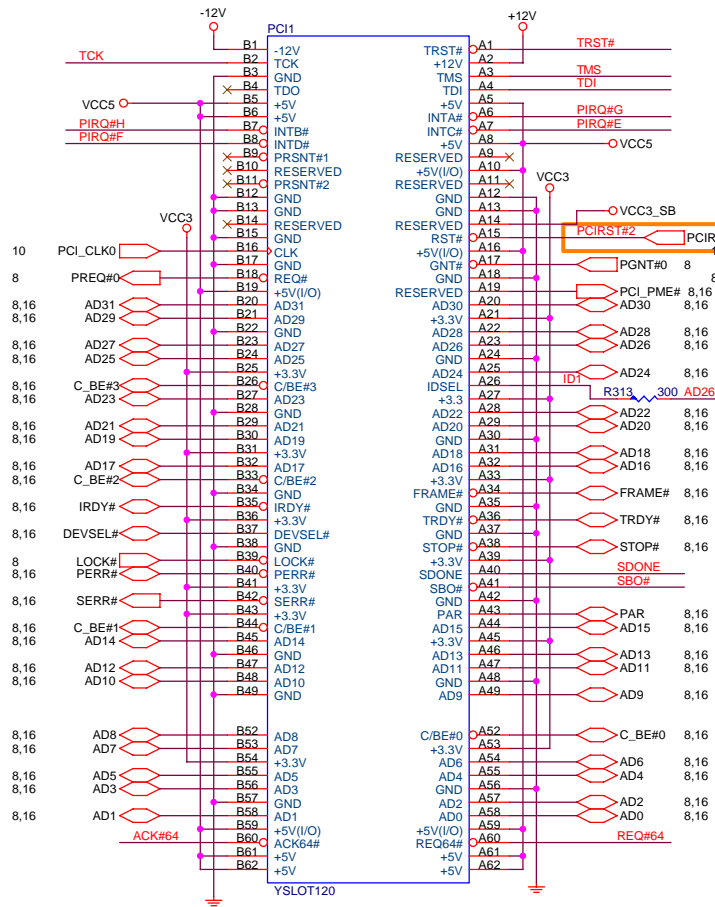




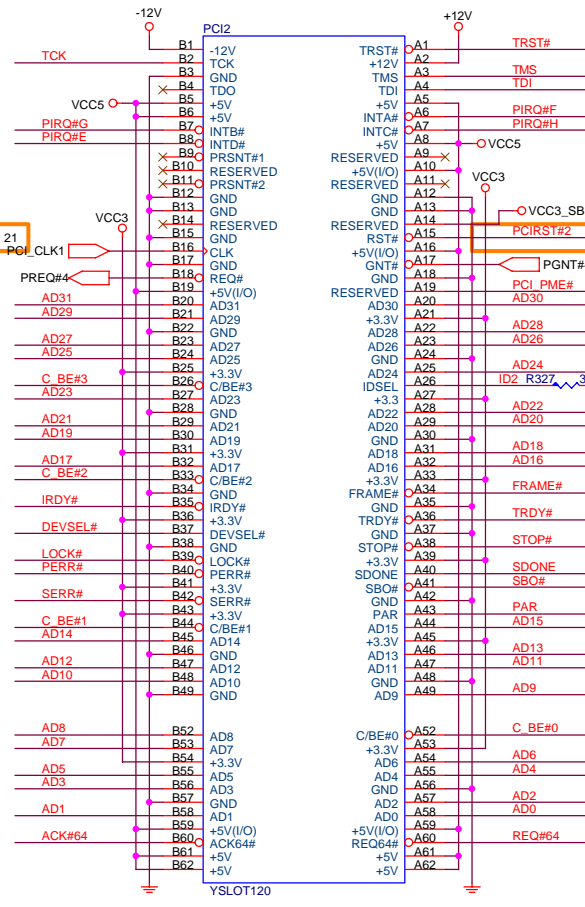
# PCI SLOT 1 (PCI VER: 2.2 COMPLY)

# PCI SLOT 2 (PCI VER: 2.2 COMPLY)

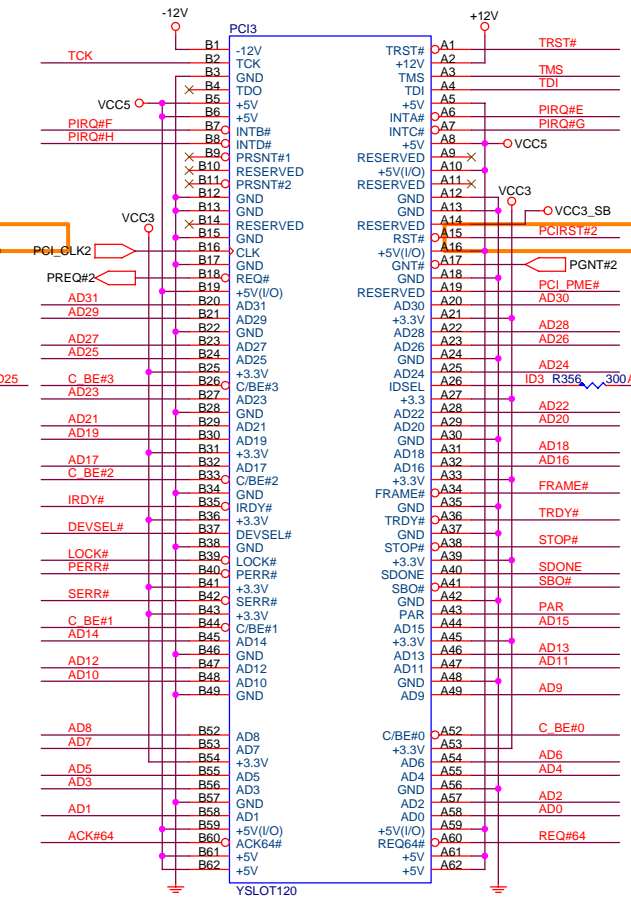
# PCI SLOT 3 (PCI VER: 2.2 COMPLY)



IDSEL = AD26  
MASTER = PREQ#0  
PIRQ#G

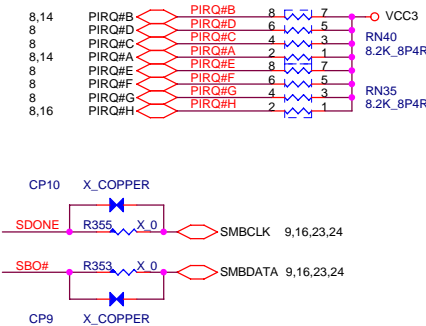
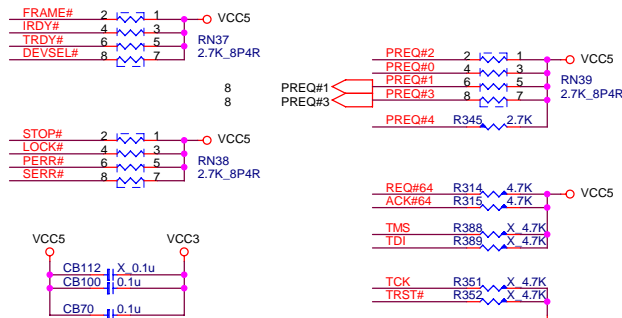


IDSEL = AD25  
MASTER = PREQ#4  
PIRQ#F

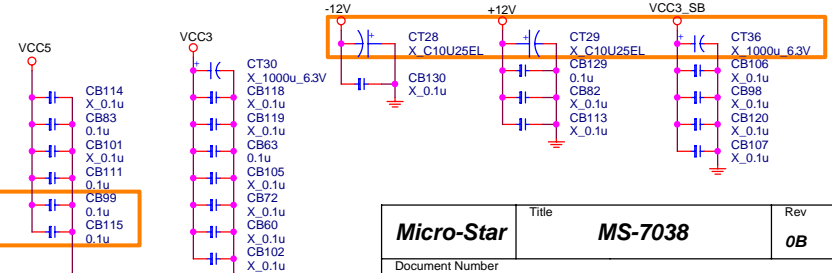


IDSEL = AD28  
MASTER = PREQ#2  
PIRQ#E

## PCI PULL-UP / DOWN RESISTORS



## PCI SLOT DECOUPLING CAPACITORS

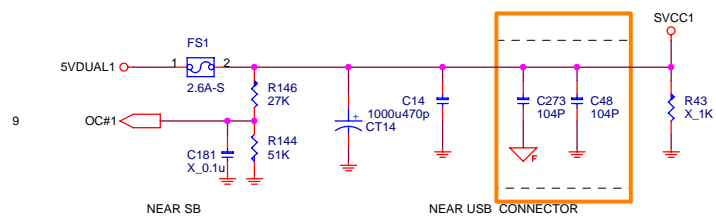


Micro-Star	Title	MS-7038	Rev	0B
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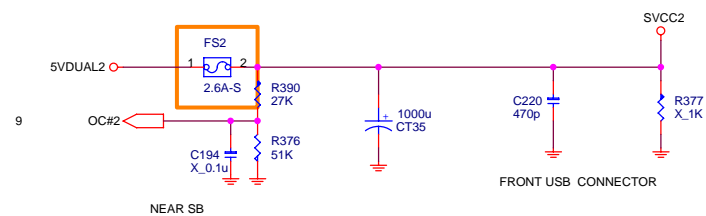




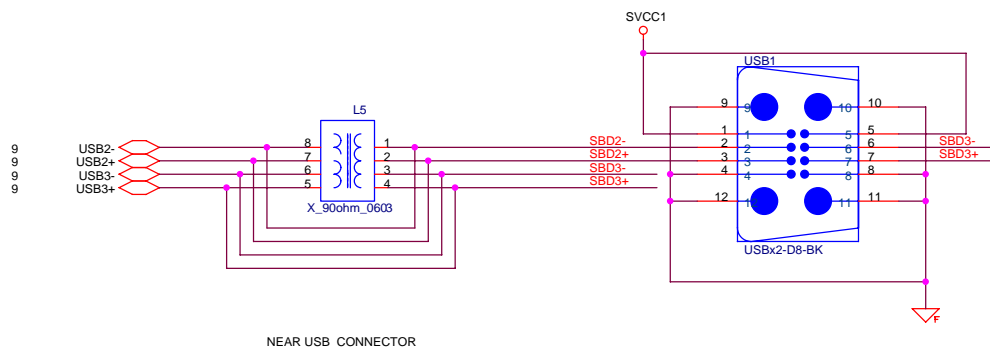
### POWER CIRCUIT FOR USB PORT 0,1,2,3



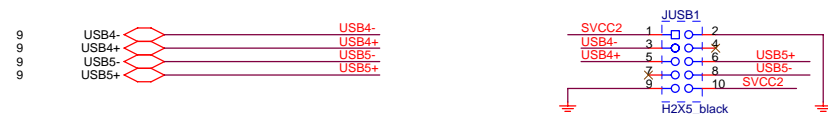
### POWER CIRCUIT FOR USB PORT 4,5,6,7



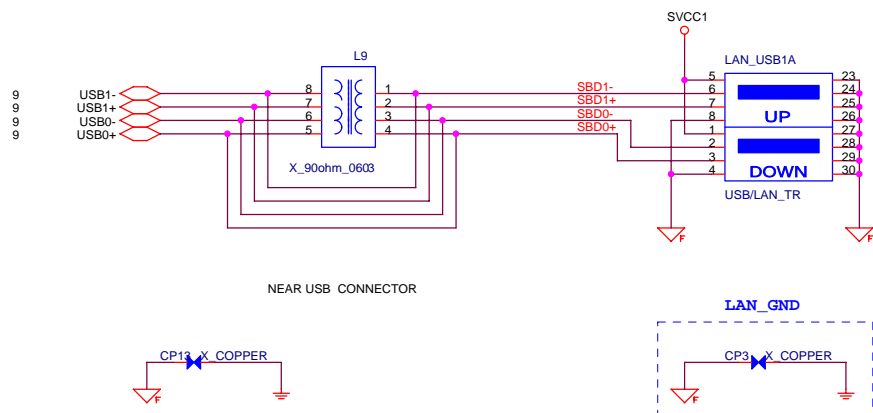
### REAR PANEL USB CONNECTOR FOR USB PORT 0,1



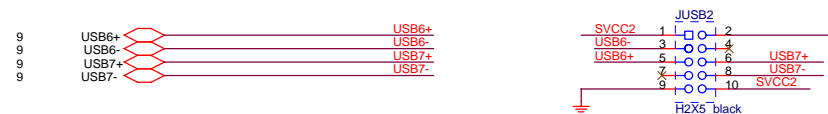
### FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



### REAR PANEL USB CONNECTOR FOR USB PORT 2,3

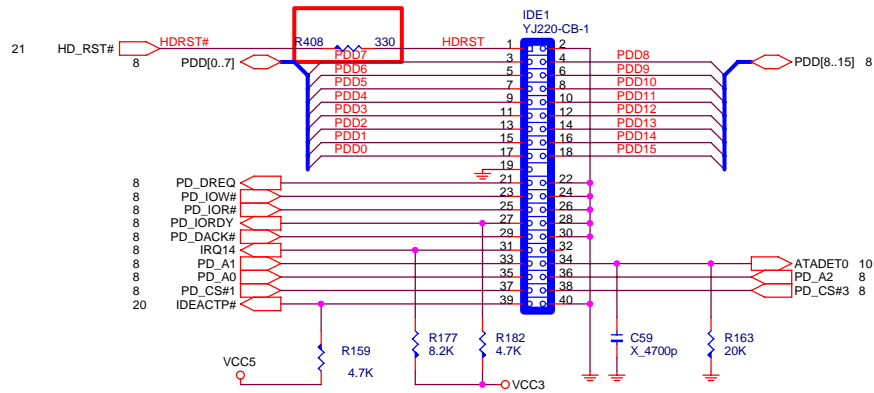


### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

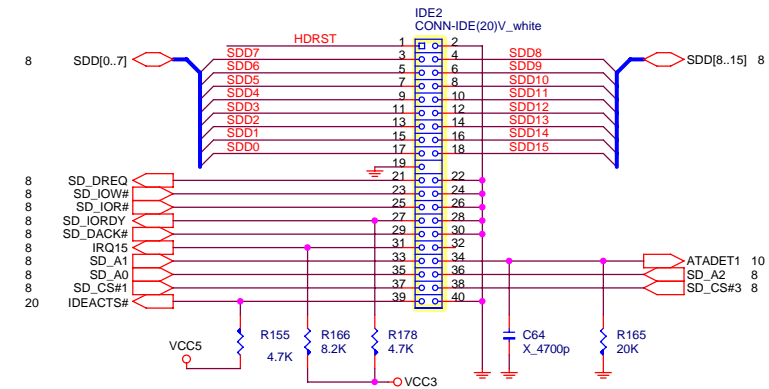


Micro-Star	Title <b>MS-7038</b>	Rev <b>0B</b>
Document Number	USB Connectors	
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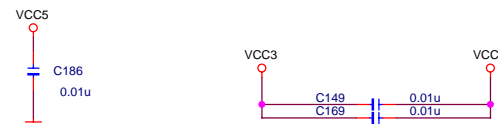
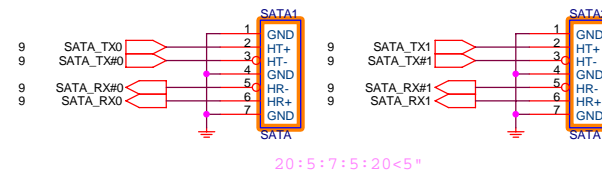
## PRIMARY IDE BLOCK



## SECONDARY IDE BLOCK

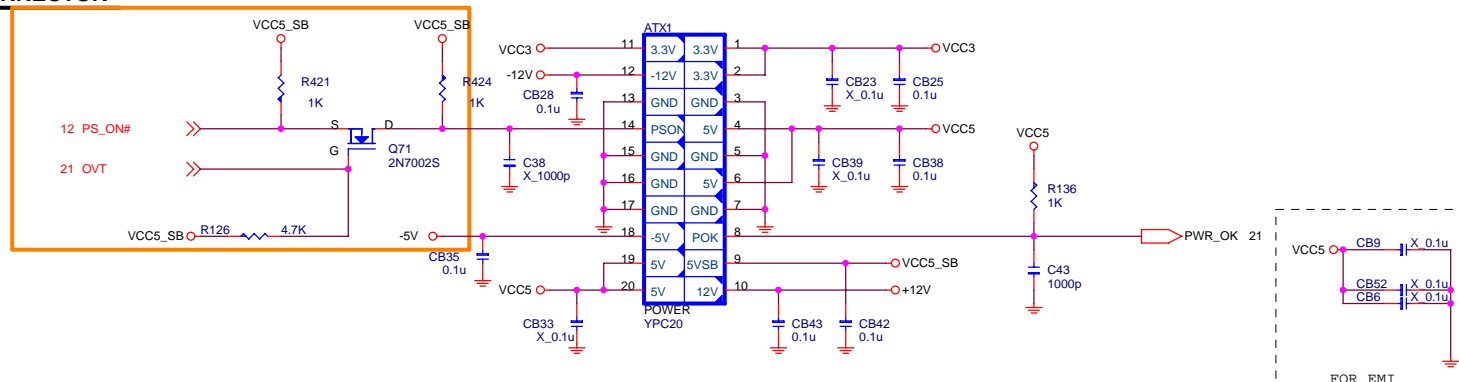


## SERIAL ATA CONNECTOR BLOCK

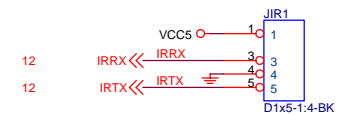


Micro-Star	Title	MS-7038	Rev 0B
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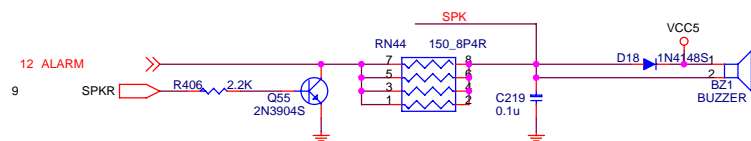
## ATX CONNECTOR



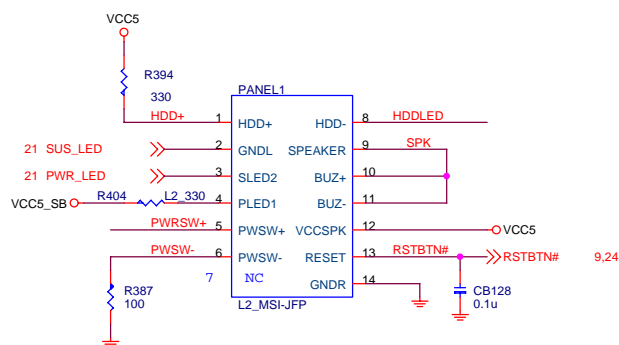
## IR CONNECT



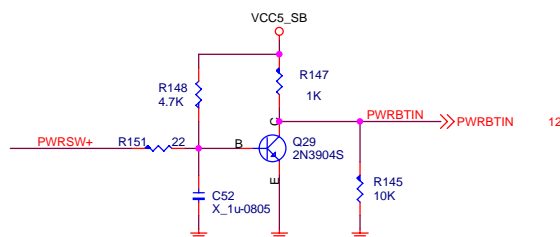
## BUZZER



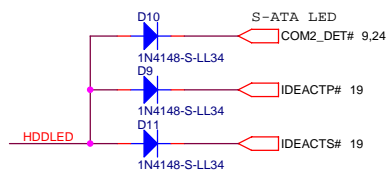
## Legend Front Panel



## POWER BUTTON



## IDE LED



Micro-Star	Title	MS-7038	Rev	0B
	Document Number	ATX, FRONT PANEL, IrDA		
Last Revision Date:		Thursday, November 27, 2003	Sheet	20 of 27

# ACPI Controller

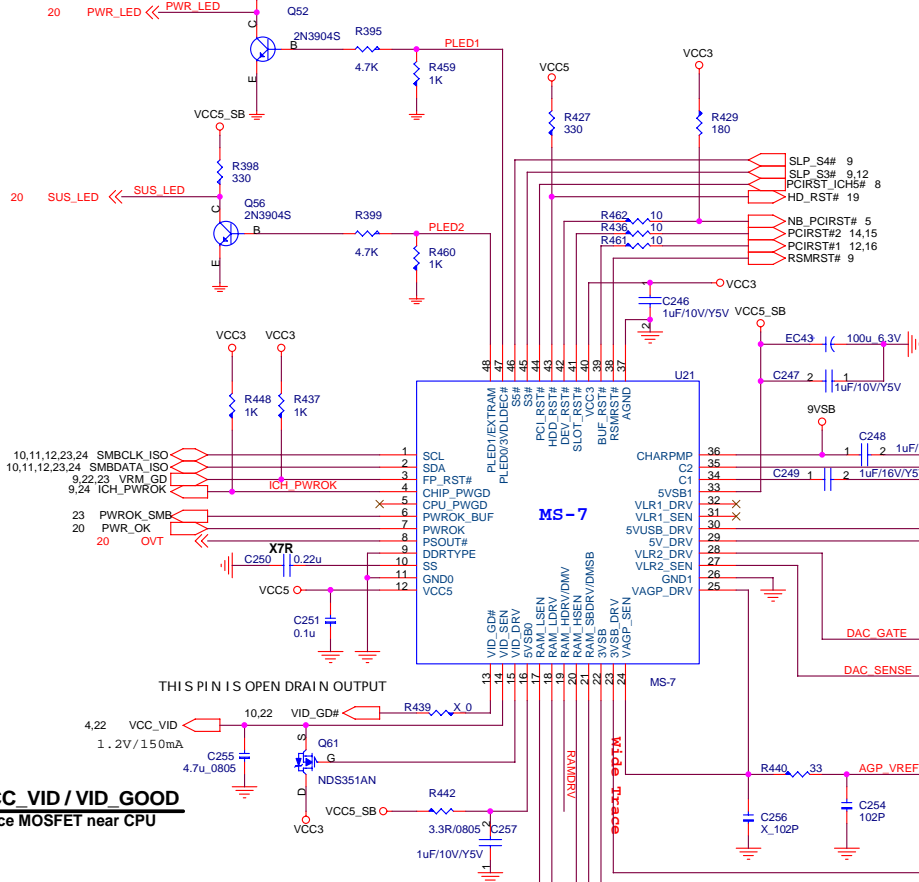
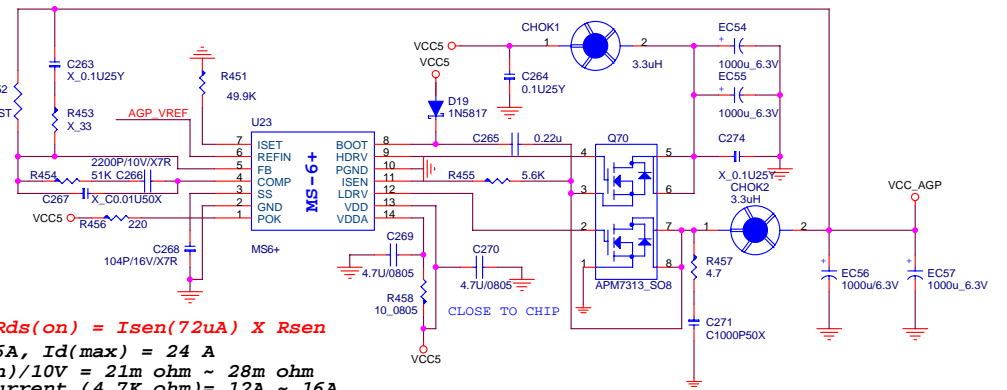
**3VSB MODE SELECT**

3VSB MODE	3VSB DECH
SINGLE MOSFET	PULL HIGH
DUAL MOSFET	PULL LOW

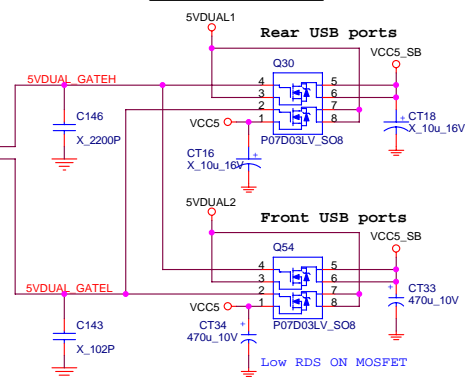
**VDIMM LINEAR OR PWM SELECT**

VDIMM MODE	EXTRAM
LINEAR REGULATOR	PULL LOW
PWM REGULATOR	PULL HIGH

## AGP POWER



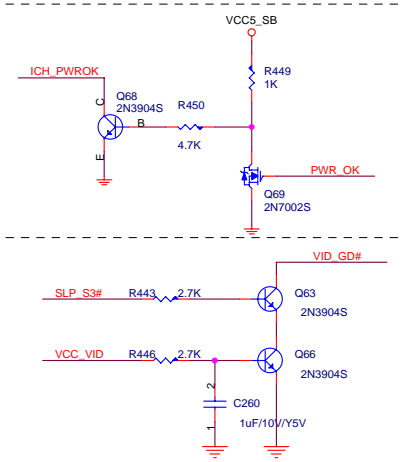
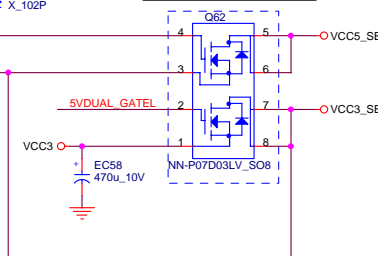
## 5V Dual Power



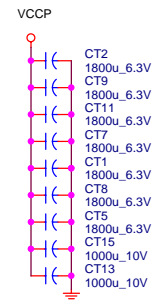
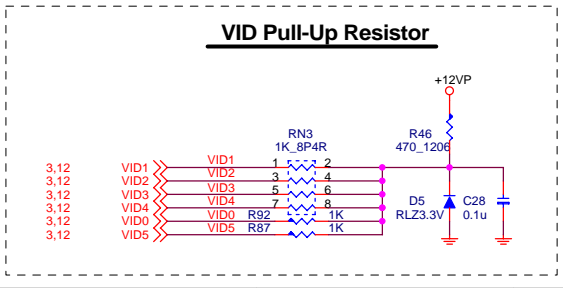
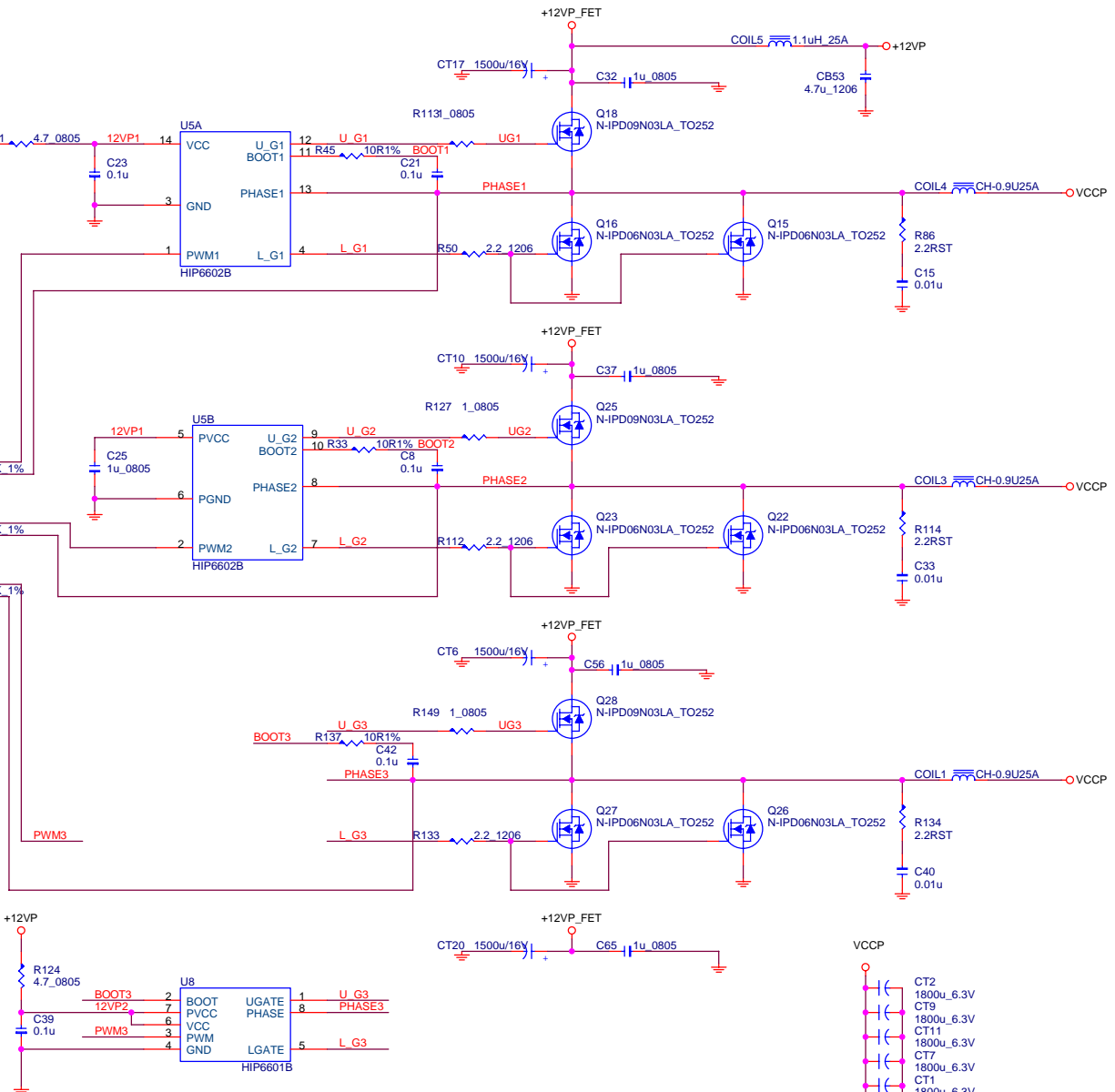
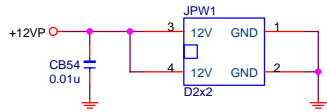
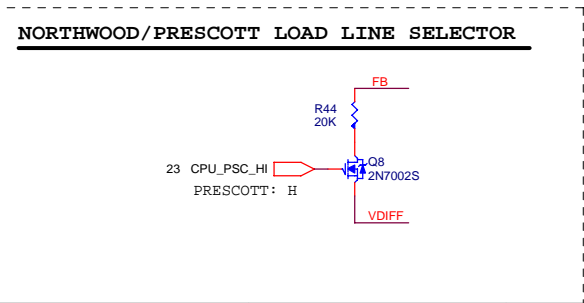
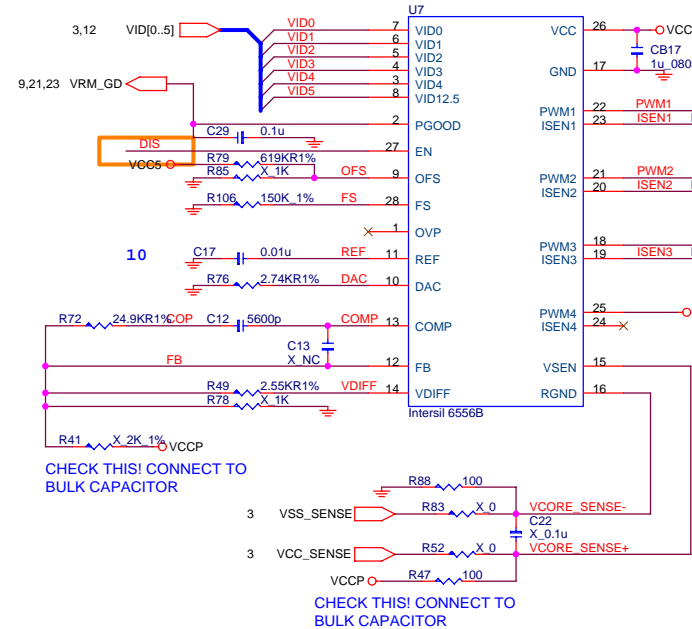
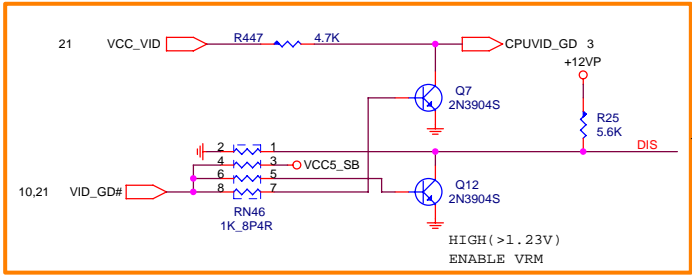
**SWITCH:**

D03-40N030B-A36  
D03-20N030B-I14  
D03-45N030B-P03  
**Regulator (TO-252)**  
D03-45N020B-N03  
D03-40N030B-A36  
D03-603AL1B-C03  
D03-6530A0B-F01  
**Regulator (TO-263)**  
D03-50N034B-N03  
D03-603AL0B-C03  
D03-703AL0B-C03

## 3V Dual Power

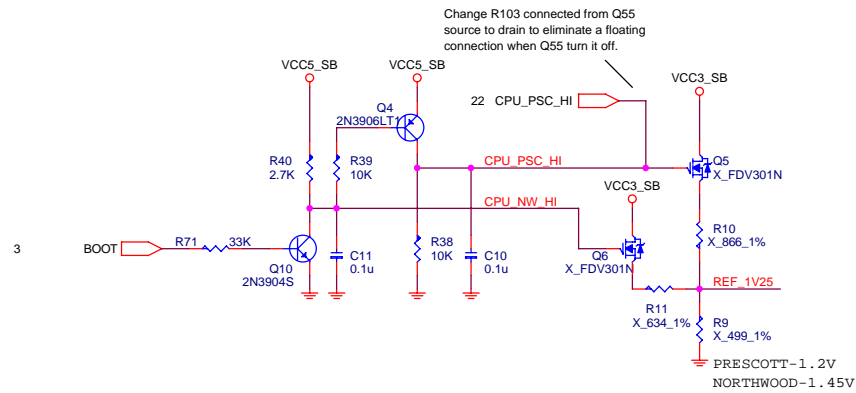


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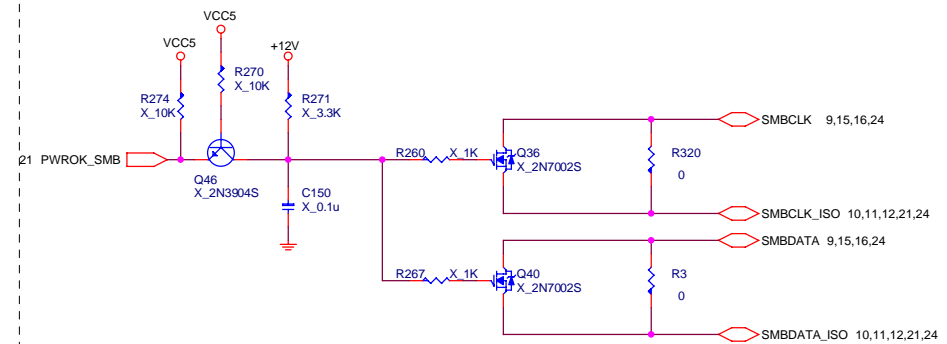
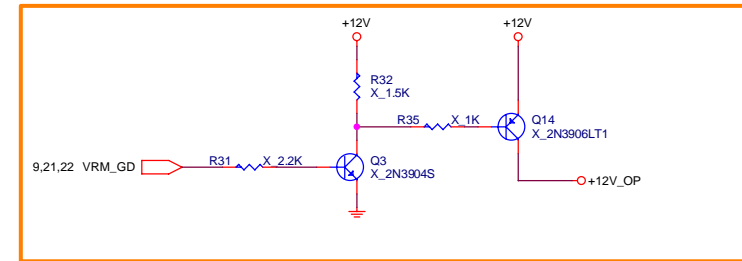


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Document Number	VRM 10 - Intersil 6556B			
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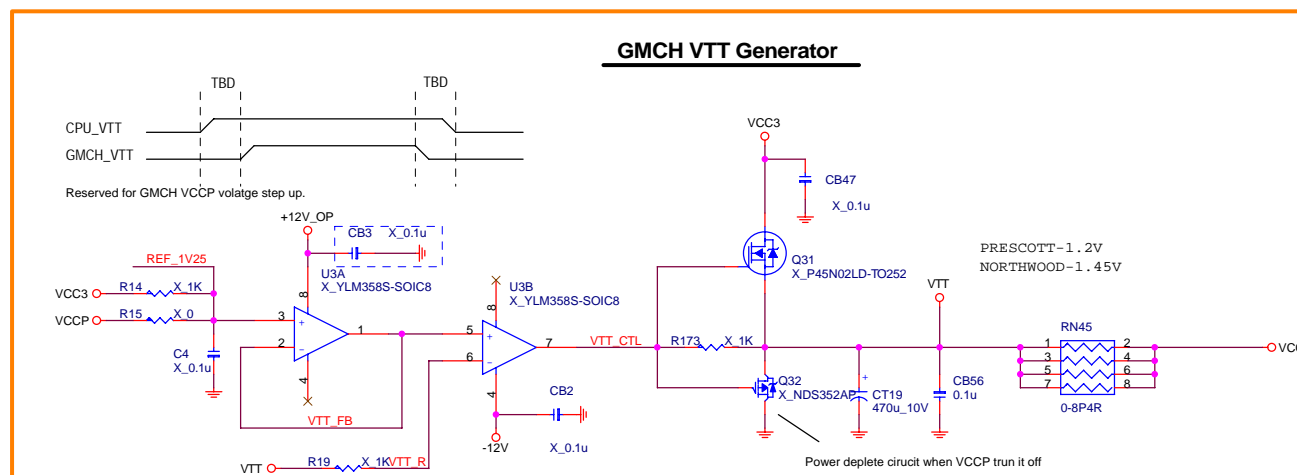
### Intel reference GMCH VTT power circuit



### GMCH\_VTT ON/OFF CIRCUIT



### GMCH VTT Generator



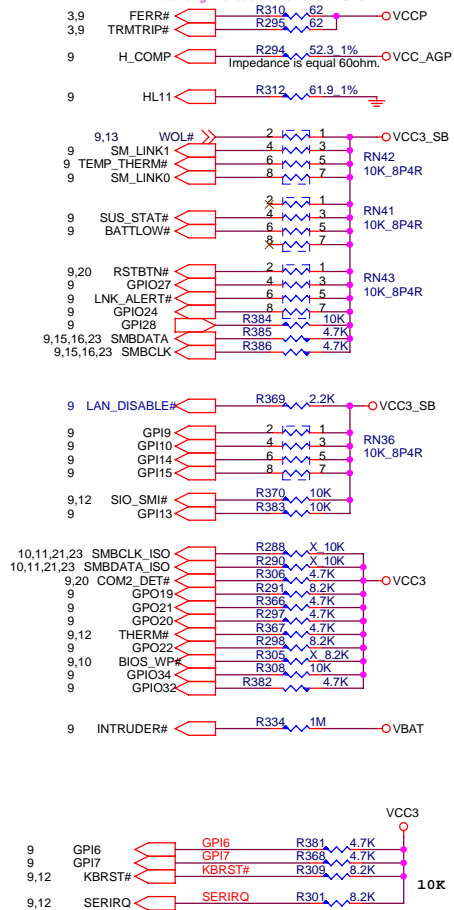
Bootstrip pin are input rather than output on Intel Prescott processor, either it's internal weak pull-up but still need to identify it can be sufficient driving capability for out side circuit. And the bootstrip pin power by core voltage so the outside circuit need to adjust the turn off voltage.

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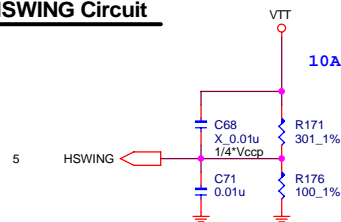
## ICH5 STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO ICH5

Trace length is less than 3inches to ICH5.



## HSWING Circuit

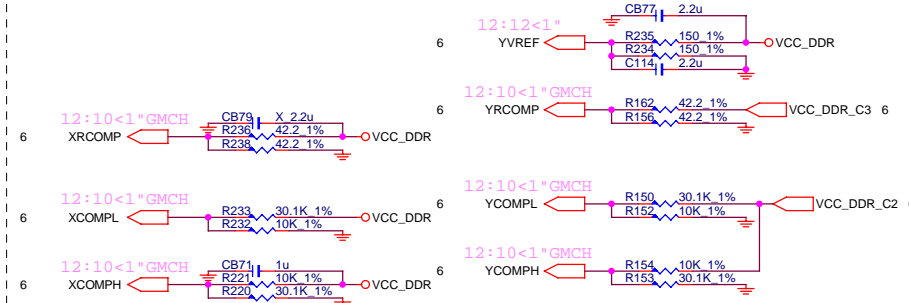
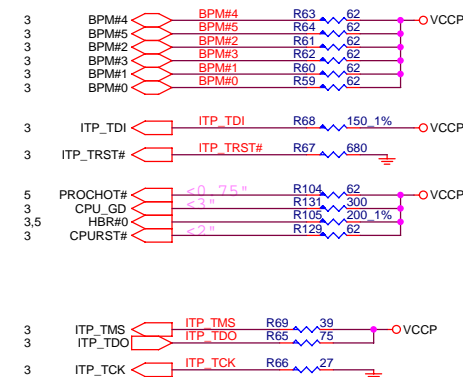


## 5VREF Sequencing Circuit



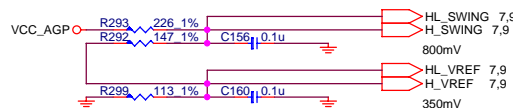
## CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU



## RTC BLOCK

CLR CMOS	
1 - 2	Normal *
2 - 3	Clear CMOS



Close to PinAD11 of ICH5.

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ICH5

GPIO Pin	Type	Function	Power well
GPIO 0	I	PREQ#A	MAIN
GPIO 1	I	PREQ#B	MAIN
GPIO 2	I	PIRQ#E	MAIN
GPIO 3	I	PIRQ#F	MAIN
GPIO 4	I	PIRQ#G	MAIN
GPIO 5	I	PIRQ#H	MAIN
GPIO 6	I	GPI6	MAIN
GPIO 7	I	GPI7	MAIN
GPIO 8	I	WOL#	RESUME
GPIO 9	I	OC4#	RESUME
GPIO 10	I	OC5#	RESUME
GPIO 11	I	TEMP_THERM#	RESUME
GPIO 12	I	SIO_SMI#	RESUME
GPIO 13	I	GPI13	RESUME
GPIO 14	I	OC#6	RESUME
GPIO 15	I	OC#7	RESUME
GPIO 16	O	PGNT#A	MAIN
GPIO 17	O	PGNT#B	MAIN
GPIO 18	O	GPO18	MAIN
GPIO 19	O	GPO19	MAIN
GPIO 20	O	GPO20	MAIN
GPIO 21	O	GPO21	MAIN
GPIO 22	OD	GPO22	MAIN
GPIO 23	O	BIOS_WP#	MAIN
GPIO 24	I/O	GPIO24	RESUME
GPIO 25	I/O	LAN_DISABLE#	RESUME
GPIO 27	I/O	GPIO27	RESUME
GPIO 28	I/O	GPIO28	RESUME
GPIO 32	I/O	GPIO32	MAIN
GPIO 33	I/O	COM2_DET#	MAIN
GPIO 34	I/O	GPIO34	MAIN
GPIO 40	I	PREQ#4	MAIN
GPIO 41	I	GPI41	MAIN
GPIO 48	O	PGNT#4	MAIN
GPIO 49	OD	CPU_GD	MAIN

default output  
default output  
default output  
default output  
default output  
default output

PCI RESET DEVICE

Signals	Target
PCIRST#1	PCI slot 1-3, LAN
PCIRST#2	Super I/O,AGP slot
PCIRST_ICH5#	Northbridge , FWH
HDDRST#	Primary, Scondary IDE

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#G PIRQ#H PIRQ#E PIRQ#F	PCI_REQ#0 PCI_GNT#0	AD26	PCICLK0
PCI Slot 2	PIRQ#F PIRQ#G PIRQ#H PIRQ#E	PCI_REQ#4 PCI_GNT#4	AD25	PCICLK1
PCI Slot 3	PIRQ#E PIRQ#F PIRQ#G PIRQ#H	PCI_REQ#2 PCI_GNT#2	AD28	PCICLK2
LAN	PIRQH	PCI_REQ#1 PCI_GNT#1	AD29	LAN_PCLK

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	AOH	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_A3/MCLK_A#3 MCLK_A4/MCLK_A#4 MCLK_A5/MCLK_A#5

JUMPER SETTING

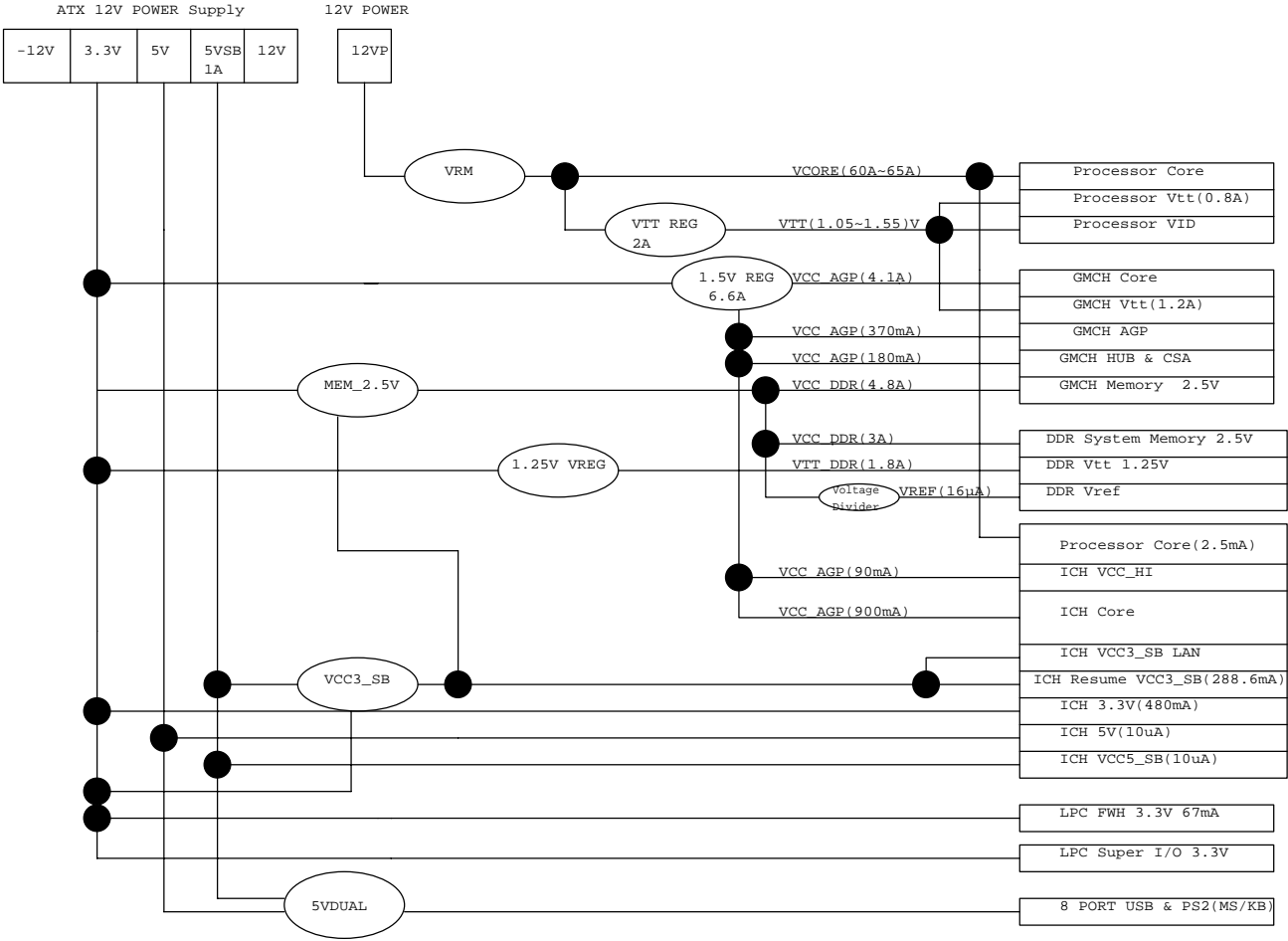
JBAT1	( 1-2 ) NORMAL	( 2-3 ) CLEAR
JAUD1	( 5-6 ) ( 9-10 ) W/O FRONT AUDIO	WITH FRONT AUDIO

SIO

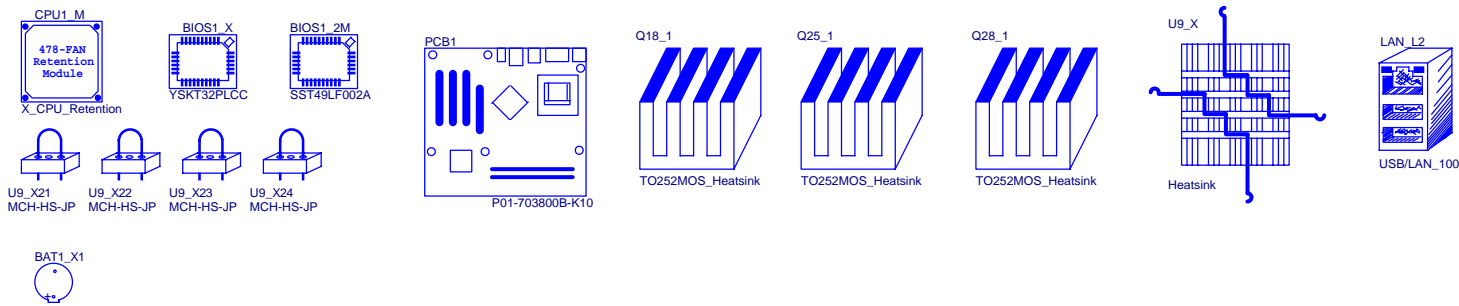
PIN NAME	USAGE	Input/Output	NOTES
GPIO10	UNUSED	INPUT	
GPIO11	UNUSED	INPUT	
GPIO12	UNUSED	INPUT	
GPIO13	UNUSED	INPUT	
GPIO14	UNUSED	OUTPUT	
GPIO15	VID5	INPUT	Low: VID add 0.0125V , High :by pass
GPIO16	UNUSED	OUTPUT	
GPIO17	UNUSED	OUTPUT	
GPIO20	UNUSED	OUTPUT	
GPIO21	SMBCLK_ISO	INPUT	SMBUS CLOCK
GPIO22	SMBDATA_ISO	INPUT / OUTPUT	SMBUS DATA
GPIO23	POWER_LED	OUTPUT	Default used MS-5
GPIO24	UNUSED	OUTPUT	
GPIO25	UNUSED	OUTPUT	IRRX
GPIO26	UNUSED	OUTPUT	
GPIO27	UNUSED	OUTPUT	
GPIO30	SLP_S3#	INPUT	S3 state indicator signal
GPIO31	PS_ON#	OUTPUT	Connector to Power Supply to turn on Power.
GPIO32	UNUSED	OUTPUT	
GPIO33	UNUSED	OUTPUT	
GPIO34	UNUSED	OUTPUT	
GPIO35	UNUSED	OUTPUT	

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POWER DELIVERY MAP



MANUAL PART



<b>Micro-Star</b>	Title <b>MS-7038</b>	Rev <b>0B</b>
Document Number <b>POWER DELIVERY MAP &amp; MANUAL PART</b>		
Last Revision Date: Wednesday, December 03, 2003		Sheet    26    of    27

# Revision History

## 0B Revision History (Changes from Rev 0A)

Sheet		Description
12		Add TPM function
14		Modify FAN speed control circuit
21		Change ACPI controller from MS-5 to MS-7
21		Change AGP power from NIKO/N2101 to MS-6+
26		Add 3 heatsink on VRM MOS